REMARKS

Upon entry of this amendment, claims 1, 3, 4 and 6-16 are all the claims pending in the application. Claims 2 and 5 have been canceled by this amendment.

I. Objections to the Specification

The Examiner has objected to the specification for the reasons set forth on page 2 of the Office Action. In particular, the Examiner has indicated that there is not proper antecedent basis for the phrase "nontamper resistant memory". By this amendment, Applicants note that this phrase has been deleted from the claims. Accordingly, Applicants kindly request that the above-noted objection be reconsidered and withdrawn.

II. Claim Rejections under 35 U.S.C. § 103(a)

A. Claims 1, 3, 6-14 and 16 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Nagamasa et al. (US 2004/0177215) in view of Kawaura (US 6,886,069); and claims 4 and 5 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Nagamasa et al. in view of Kawaura, and further in view of Madoukh (US 2001/0019614).

By this amendment, Applicants note that claim 1 has been amended so as to include all of the features recited in claim 5, and claim 5 has been canceled.

Regarding claim 1, Applicants note that this claim recites the features of a tamper resistant module that includes an internal memory having a usage area used by a program stored in the tamper resistant module; and a processing unit, wherein when requested by the program, the processing unit is operable to (i) assign an area in the nonvolatile memory that is not tamper

resistant to the program, and (ii) generate, in the internal memory of the tamper resistant module, access information for the assigned area in the nonvolatile memory that is not tamper resistant.

Regarding the above-noted features, Applicants note that the Examiner has taken the position in the Office Action that Nagamasa discloses such features. In particular, the Examiner has indicated that, in Nagamasa, the EEPROM 162 of the IC card chip 150 corresponds to the claimed "internal memory", and that the flash memory chip 130 corresponds to the claimed 'non-volatile memory" (see Office Action at pages 3-4).

Taking into account the above-noted features recited in claim 1, as well as the Examiner's above-noted correspondence between the elements in Nagamasa and the features recited in claim 1, Applicants note that the Examiner has taken the position that access information for an area of the flash memory chip 130 is generated in the EEPROM 162. Applicants respectfully disagree.

With respect to the above-noted argument, Applicants note that the same argument was presented in the previous response, and in response to this argument, the Examiner has stated in the present Office Action that the "examiner maintains that data is stored on the IC card chip 150 on EEPROM 162 as stated in the rejection of record" (see Office Action at page 11). In response to this comment made by the Examiner, Applicants respectfully point out that the Examiner has not addressed the argument.

In particular, Applicants note that it has not been argued that the EEPROM 162 of Nagamasa does not store data thereon. Instead, as set forth in the previous response, as well as the comments above, Applicants submit that Nagamasa does not disclose or in any way suggest

the ability to generate, in the EEPROM 162, access information for an area of the flash memory chip 130.

If the Examiner disagrees, Applicants kindly request that the Examiner specifically identify the information in Nagamasa that is being relied upon as corresponding to the claimed "access information" that is generated in the EEPROM 162 so that Applicants can make an informed decision with regard to appeal.

In view of the foregoing, Applicants respectfully submit that Nagamasa does not disclose, suggest or otherwise render obvious at least the above-noted features recited in claim 1 of a tamper resistant module that includes an internal memory having a usage area used by a program stored in the tamper resistant module; and a processing unit, wherein when requested by the program, the processing unit is operable to (i) assign an area in the nonvolatile memory that is not tamper resistant to the program, and (ii) generate, in the internal memory of the tamper resistant module, access information for the assigned area in the nonvolatile memory that is not tamper resistant. Further, Applicants respectfully submit that Kawaura and Madoukh do not cure this deficiency of Nagamasa. Accordingly, Applicants submit that claim 1 is patentable over the cited prior art, an indication of which is kindly requested.

In addition, Applicants note that claim 1, as amended herein, also recites that the access information is a set of the predetermined encryption key and information indicating a location of the second area table. Applicants respectfully submit that the cited prior art references do not teach or suggest the above-noted feature.

In particular, with respect to the above-noted feature, Applicants note that the Examiner

has taken the position that, in Nagamasa, the claimed "access information" is stored on the EEPROM 162, and that the claimed "second area table" is stored on the flash memory chip 130. In addition, regarding the claimed "predetermined encryption key", Applicants note that the Examiner has relied on Madoukh for the teaching of an encryption key manager, and has taken the position that it would have been obvious to modify the semiconductor card as taught by Nagamasa and Kawaura with the encryption methods as taught by Madoukh (see Office Action at page 9).

Regarding such a position, Applicants respectfully submit that even if the encryption methods of Madoukh were applied to the semiconductor card as taught by Nagamasa and Kawaura, that there would still be no teaching or suggestion of storing, on the EEPROM 162 of Nagamasa, information indicating a location of a second area table that is stored in the flash memory chip 130. In particular, Applicants note that if the encryption methods of Madoukh were somehow applied to Nagamasa and Kawaura, that while such a combination may result in a semiconductor memory card having the ability to encrypt and decrypt the contents stored therein, that such a combination would not in any way whatsoever result in data being stored on the EEPROM 162 of Nagamasa that indicates a location of a second area table stored in the flash memory chip 130.

If the Examiner disagrees, Applicants kindly request that the Examiner specifically explain how the encryption methods of Madoukh would result in data being stored on the EEPROM 162 of Nagamasa that indicates a location of a second area table stored in the flash memory chip 130.

In view of the foregoing, Applicants respectfully submit that the cited prior art references do not disclose, suggest or otherwise render obvious the above-noted feature recited in amended claim 1 which sets forth that the access information is a set of the predetermined encryption key and information indicating a location of the second area table. Accordingly, Applicants submit that claim 1 is patentable over the cited prior art, an indication of which is kindly requested.

Regarding claims 3, 4 and 6-14, Applicants note that these claims depend from claim 1 and are therefore considered patentable at least by virtue of their dependency.

Regarding claim 16, Applicants note that this claim has been amended in a similar manner as claim 1. In particular, claim 16 recites that the tamper resistant module includes an internal memory having a usage area used by an application stored in the tamper resistant module; that the controlling program is operable to (i) assign an area in the nonvolatile memory that is not tamper resistant to the application, and (ii) generate, in the internal memory of the tamper resistant module, access information for the assigned area in the nonvolatile memory that is not tamper resistant; wherein the access information is a set of the predetermined encryption key and information indicating a location of the second area table.

For at least similar reasons as discussed above with respect to claim 1, Applicants respectfully submit that the cited prior art references do not teach, suggest or otherwise render obvious such a combination of features. Accordingly, Applicants submit that claim 16 is patentable over the cited prior art, an indication of which is kindly requested.

B. Claim 15 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Nagamasa et al. (US 2004/0177215) in view of Kawaura (US 6,886,069), and further in view of Deo et al. (US 5,721,781).

Claim 15 depends from claim 1. For the reasons discussed above, Applicants respectfully submit that Nagamasa, Kawaura and Madoukh do not teach, suggest or otherwise render obvious all of the features recited in claim 1. Further, Applicants respectfully submit that Deo fails to cure these deficiencies of Nagamasa, Kawaura and Madoukh. Accordingly, Applicants submit that claim 15 is patentable at least by virtue of its dependency.

III. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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